

AN1077: Selecting the Right Clocks for Timing Synchronization Applications

Today's ever-increasing demands for network bandwidth are driving data rates higher, while increasing demand for network frequency and phase synchronization with GPS and IEEE 1588. To meet the timing requirements of the latest high-bandwidth networks, clock and timing sources must have extremely low jitter while simultaneously supporting low PLL bandwidths down to 0.001 Hz. Skyworks' DSPLL family is uniquely designed to meet both of these requirements. This document outlines clock tree considerations that must be made for the latest applications in optical and wireless communications, while providing guidance to help select the appropriate Skyworks timing devices.

KEY POINTS

- Introduces jitter and wander requirements for timing synchronization applications
- Explains phase noise, jitter, and wander considerations for single-reference and dual-reference clocks
- Discusses recommended DSPLL devices for various timing architectures
- Shows synchronization clock selection guide

1. Jitter vs. Wander

To meet the synchronization clocking needs of standards such as SyncE, SONET/SDH and IEEE 1588, both jitter and wander must be minimized. As defined by ITU-T, jitter is the phase variation in a clock signal with frequency components greater than 10 Hz offset from the carrier frequency. Conversely, wander is the phase variation in a clock signal with frequency components less than 10 Hz offset from the carrier frequency. The phase noise plot below from a Si5348 device identifies the wander and jitter components.

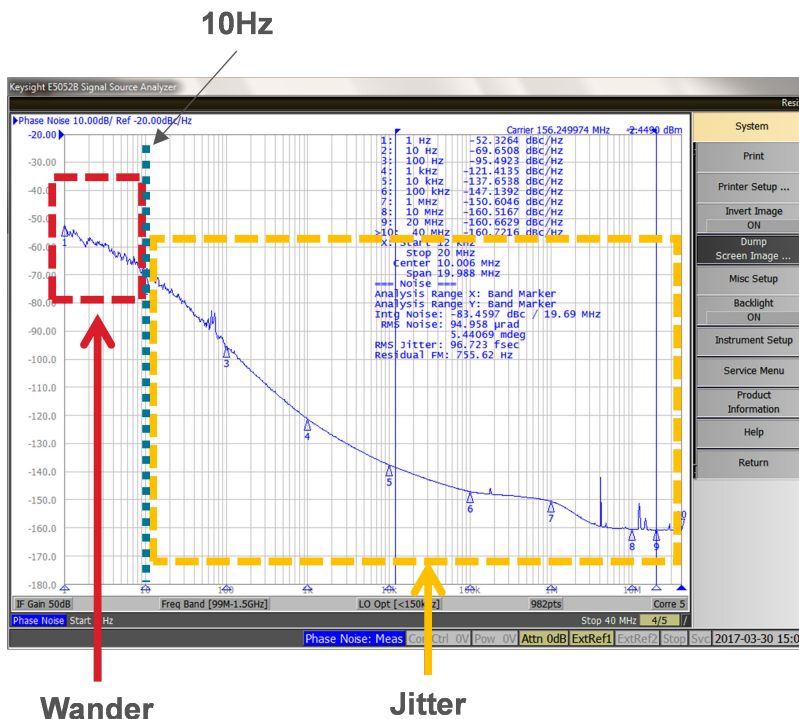


Figure 1.1. Si5348 Phase Noise, Jitter and Wander

Note that when comparing specifications for jitter, the integration range must be specified. The industry and Skyworks use the range from 12 kHz to 20 MHz to specify jitter for Si534x/8x devices. High-speed SerDes devices typically have a jitter specification that must be met in order to achieve desired bit error rate limits.

Wander can be measured using Maximum Time Interval Error (MTIE) and Time Deviation (TDEV) methods. Standards such as ITU-T G.8262 (SyncE) specify limits for MTIE and TDEV that must be met in order to achieve compliance.

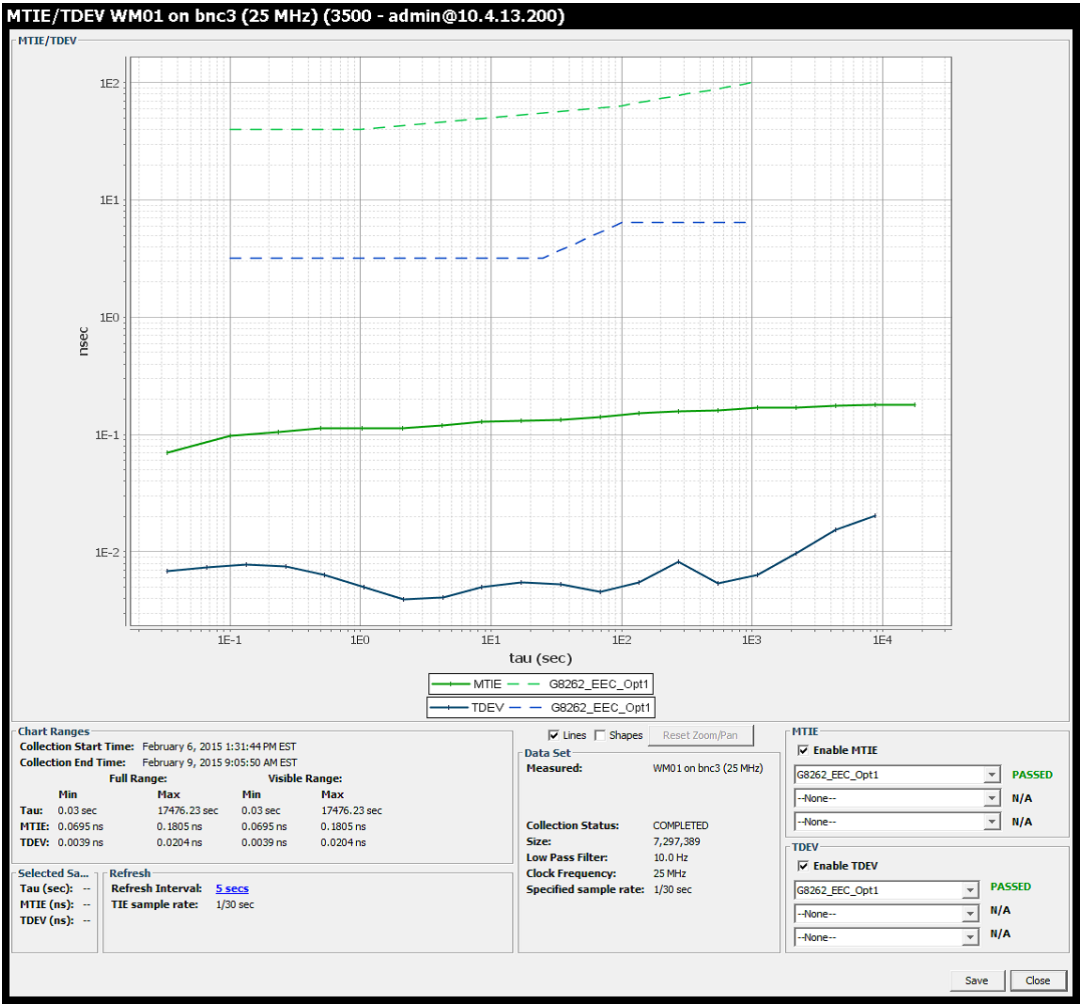


Figure 1.2. Si5348 MTIE/TDEV Performance vs. G.8262 Limits

2. Phase Noise, Jitter and Wander in Si534x Single-Reference Clocks

2.1 Single-Reference Jitter Attenuating Clock Definition

Skyworks products such as Si5342/4/5/6/7 are considered to be “single reference” jitter attenuating clocks since they have one input for either a crystal or oscillator connected to the XA/XB pins. The reference input determines the frequency stability of the device and also determines the phase noise performance at offset frequencies above the PLL bandwidth.

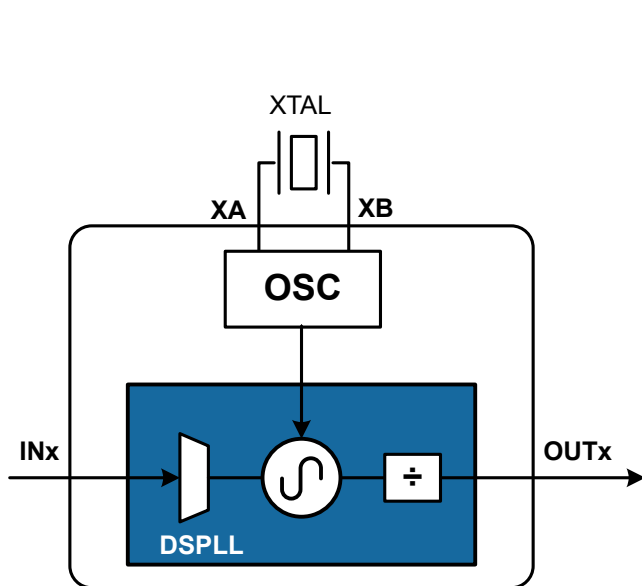


Figure 2.1. Si534x Single-Reference Jitter Attenuating Clock with Crystal Input

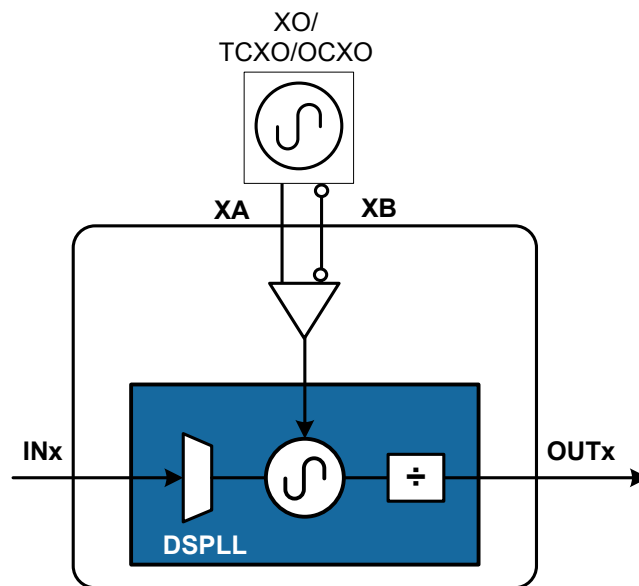


Figure 2.2. Si534x Single-Reference Jitter Attenuating Clock with Oscillator Input

2.2 Single-Reference Clock Phase Noise with Crystal Input

Single-reference jitter attenuating clocks will attenuate phase noise that exists above the chosen PLL bandwidth. Therefore if a bandwidth above 10 Hz is used, the device will attenuate jitter only. If a bandwidth below 10 Hz is used, the device will attenuate both wander and jitter. The magnitude of attenuation is determined by transfer function of the PLL, thus the attenuation is greater at higher frequency offsets from the PLL bandwidth. Sources of phase noise in these types of clocks are summarized below:

- Above the PLL bandwidth, phase noise from the input clock is attenuated. Output clock phase noise is dominated by the quality of the reference crystal, oscillator circuit and VCO.
- Below the PLL bandwidth, there is no phase noise attenuation. Therefore the phase noise of the input clock is added to the phase noise floor from the oscillator circuit and VCO.

The following figure illustrates the sources of phase noise from a single-reference clock using a PLL bandwidth of 1 kHz:

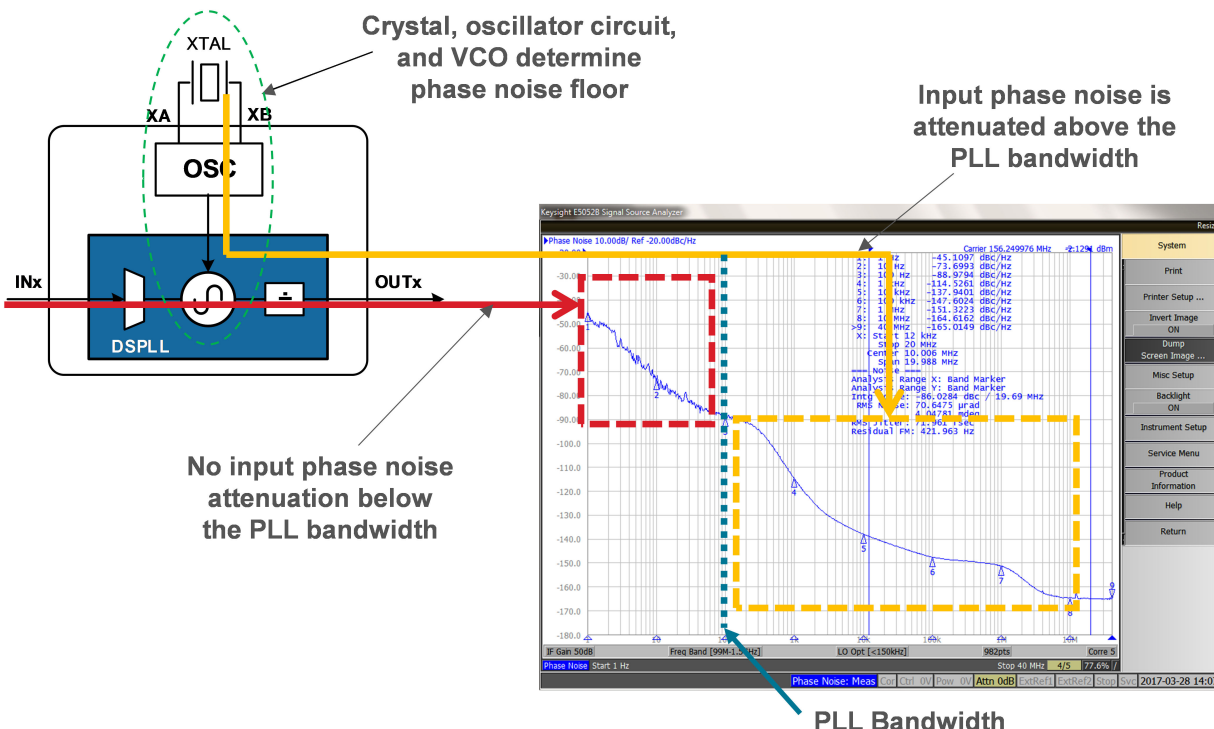


Figure 2.3. Phase Noise Measured from Single-Reference Clocks with Crystal

2.3 Single-Reference Clock Phase Noise with Oscillator Input

An oscillator, TCXO or OCXO may be connected to the XA/XB reference input on Si534x devices in lieu of a crystal. In this case, the oscillator connected to XA/XB will determine the phase noise floor above the PLL bandwidth. Therefore the following recommendations should be followed if it is desired to have low-jitter output clocks from Si534x when an oscillator is connected to the XA/XB pins:

- A low-phase noise oscillator must be used
- The clock output from the oscillator should have reasonably fast slew rates. For best performance, do not use device with a clipped-sine wave output. Instead, an oscillator with a CMOS output is recommended.

It should be emphasized that the jitter performance of most commercial oscillators will not match the jitter performance of the Si534x. For the best jitter performance, Skyworks recommends using a crystal with single-reference clocks, or using one of the dual-reference clocks described in the sections below.

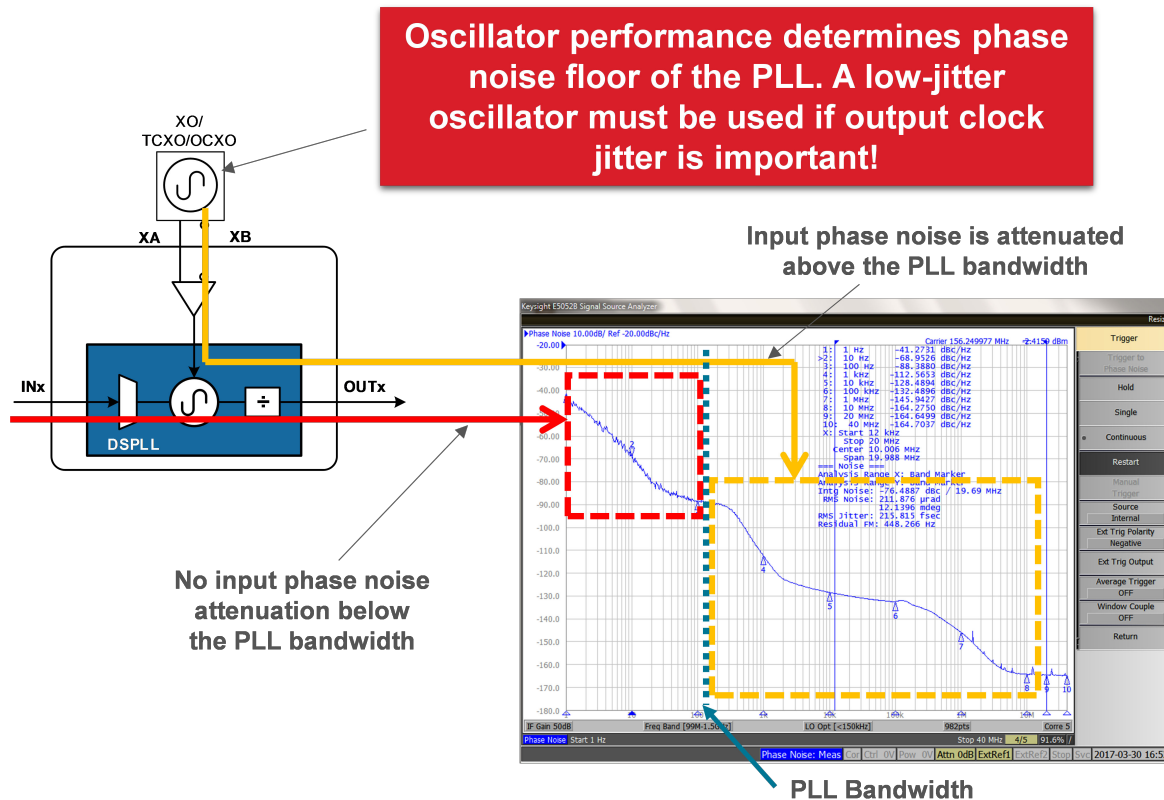


Figure 2.4. Phase Noise Measured from Single-Reference Clocks with Oscillator

When using an oscillator connected to the XA/XB pins, be sure to check the Si534x datasheet limits for minimum and maximum input frequency to be sure the oscillator's output frequency can be supported.

2.4 Wander Generation from Single-Reference Clocks

For bandwidths below 40 Hz, crystals can produce large phase noise transients caused by temperature variation and physical vibration. These transients will result in poor output clock phase noise performance at offset frequencies below 40 Hz, as well as poor MTIE/TDEV performance. This is sometimes referred to as “crystal wander generation” even though it affects jitter above 10 Hz as well. This is illustrated in the figure below:

Phase Noise Transients from Vibration and Temperature Variation

Expected Output Clock Phase Noise

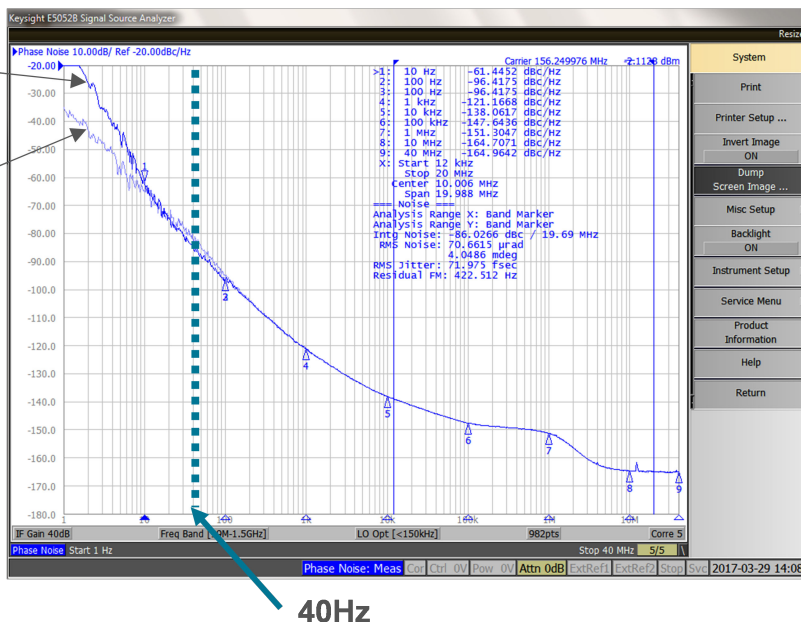


Figure 2.5. Phase Noise Performance with Crystal on XA/XB and Bandwidth <40 Hz

For these reasons, when using a single-reference jitter attenuating clock with a PLL bandwidth below 40 Hz for SyncE, SONET/SDH and IEEE 1588 applications, Skyworks recommends that a TCXO or OCXO be connected to the XA/XB pins instead of a crystal or XO. The TCXO or OCXO will not exhibit these same phase noise transients.

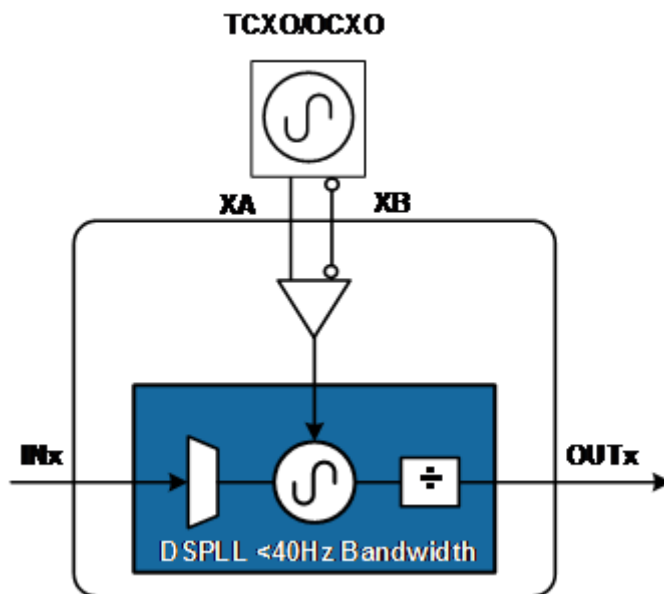


Figure 2.6. TCXO or OCXO Recommended for Bandwidths <40 Hz

2.5 Holdover Frequency Averaging in Single-Reference Clocks

For applications including SyncE, SONET and SDH that require a PLL to enter holdover when a clock becomes invalid, the Si534x devices offer historical frequency averaging to calculate the initial frequency offset during entry into holdover. The holdover circuit for each DSPLL inside the Si534x stores up to 120 seconds of historical frequency data while locked to a valid clock input. This data uses the XA/XB input as its reference. When entering holdover, the DSPLL will then pull its output clock frequency to the calculated average historical frequency. This removes static frequency offsets that exist on the local oscillator connected to XA/XB, which provides greater holdover accuracy.

In applications where a TCXO or OCXO is used with Si5342/4/5/6/7 single-reference clocks, the TCXO/OCXO must be connected to the XA/XB reference input and NOT connected to a spare PLL input. Although it is possible to configure the Si534x to automatically switch between clock inputs when one fails, connecting the TCXO/OCXO to a free PLL input has the following drawbacks:

- The holdover frequency averaging feature will not be available to provide a frequency offset during entry into holdover. This will make it difficult to meet the holdover accuracy requirements for SyncE/SONET/SDH and may result in large output clock phase transients when entering and exiting holdover.
- If the PLL bandwidth is below 40 Hz, wander performance will be poor due to the wander generation from the crystal (see previous section)
- Applying a TCXO/OCXO a clock input reduces the number of inputs available for other clocks

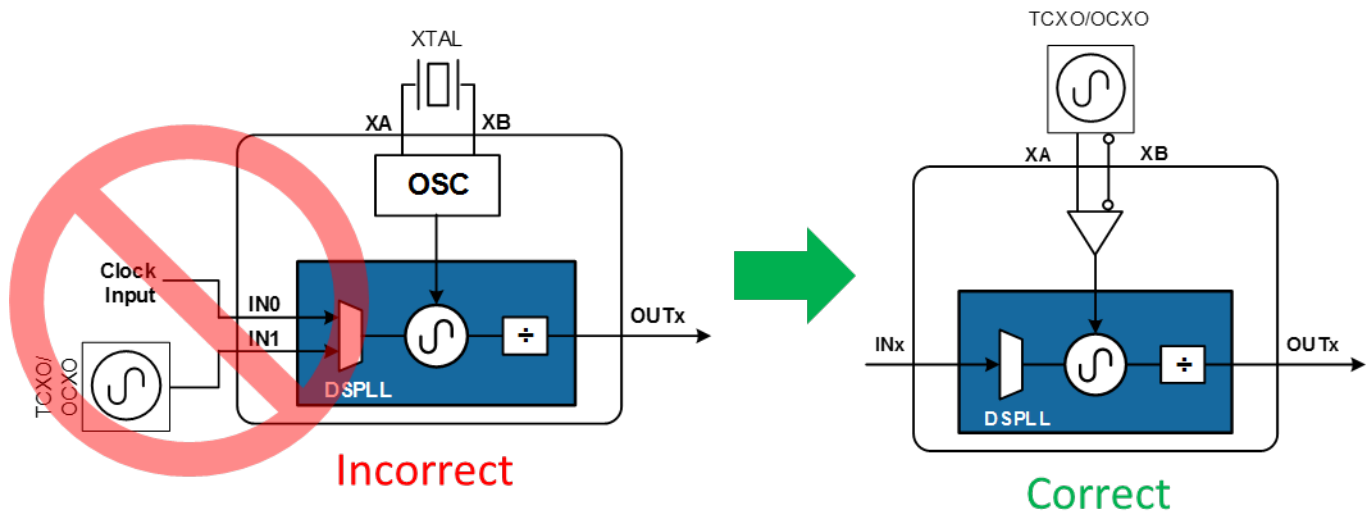


Figure 2.7. TCXO/OCXO Connection to Si5342/4/5/6/7 for Holdover Support in SyncE/SONET/SDH

3. Phase Noise, Jitter and Wander in Skyworks Dual-Reference Clocks

3.1 Dual-Reference Network Synchronizer Clock Definition

Skyworks products like the Si5348/83/84 are considered to be “dual reference” clocks since they have two inputs for a crystal and oscillator – one connected to the XA/XB pins and another connected to the REF/REFb pins. A crystal is connected to the XA/XB pins and this determines the jitter performance of the device at offsets above 100 Hz. A TCXO or OCXO is typically connected to the REF/REFb pins and this determines both the frequency stability of the device as well as the jitter and wander performance below 100 Hz. These devices are typically used for network synchronization applications such as SyncE and SONET/SDH.

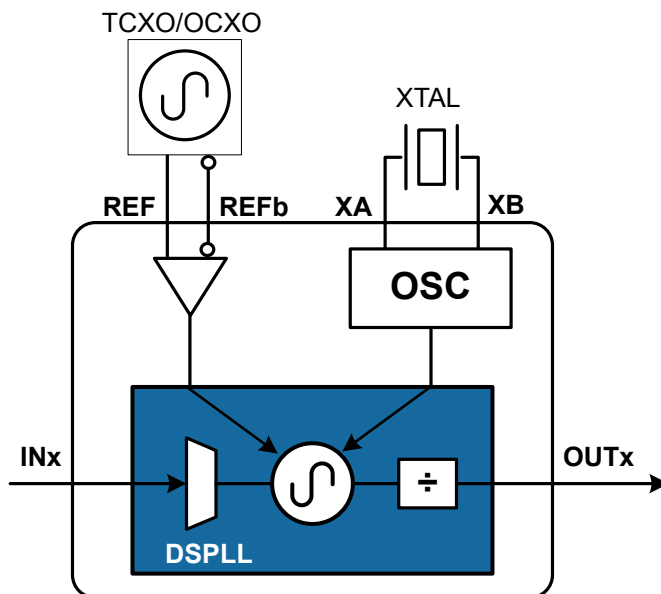


Figure 3.1. Si5348/83/84 Dual-Reference Network Synchronizer Clock

3.2 Dual-Reference Clock Phase Noise with Crystal and TCXO/OCXO Inputs

Unlike those of competitors, Skyworks' dual-reference clocks offer the advantage of using a TCXO/OCXO to provide frequency stability without the TCXO/OCXO affecting the 12 kHz to 20 MHz jitter performance of the device. Sources of phase noise in these types of devices are divided into three categories:

- Above 100 Hz, phase noise from the input clock is attenuated. Output clock phase noise is dominated by the quality of the reference crystal, oscillator circuit and VCO.
- Between the PLL bandwidth and 100 Hz, phase noise from the input clock is also attenuated. However the output clock phase noise is primarily determined by the phase noise of the TCXO/OCXO connected to the REF/REFb pins and the VCO.
- Below the PLL bandwidth, there is no phase noise attenuation. Therefore the phase noise of the input clock is added to the phase noise floor from the VCO.

This is illustrated in [Figure 3.2 Phase Noise Measured from Dual-Reference Clocks on page 10](#).

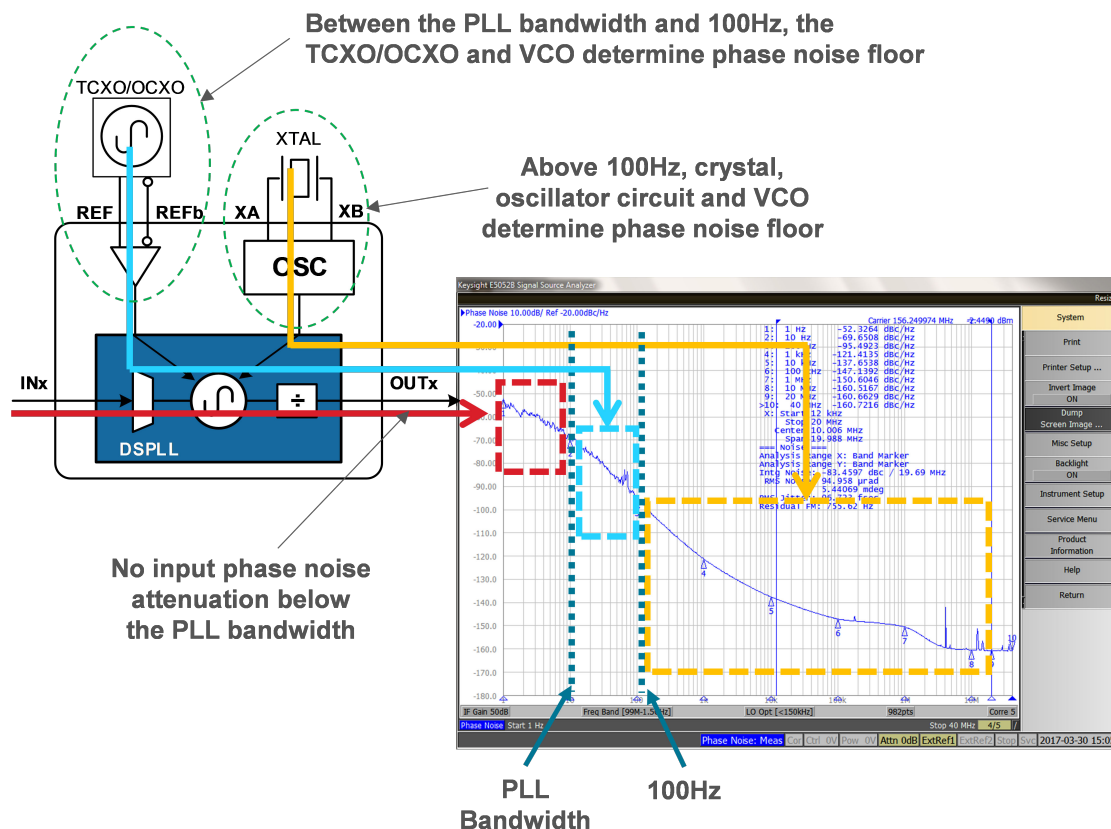


Figure 3.2. Phase Noise Measured from Dual-Reference Clocks

Although two external components are required, the dual-reference clocks offer the following advantages over the single-reference clocks:

- Jitter above 100 Hz is not affected by the TCXO/OCXO. Therefore an additional jitter attenuator is not required on the PCB to provide low-jitter clocks for SerDes and other components.
- Below 100 Hz, the PLL takes advantage of the low jitter and wander from the TCXO/OCXO reference, and the TCXO/OCXO provides a stable reference for holdover.
- A wide range of TCXO/OCXO output frequencies are supported: 5 to 250 MHz
- Skyworks' dual-reference clocks support 1 PPS/1 Hz frequencies

3.3 Holdover Frequency Averaging in Dual-Reference Clocks

Skyworks' dual-reference clocks use the REF/REFb reference input (not the XA/XB input) as the reference for holdover frequency averaging. Therefore, the calculated frequency offsets for holdover entry will use the stable TCXO/OCXO reference.

4. Recommended DSPLL Devices for Various Timing Architectures

4.1 Distributed Timing Architecture

High-performance telecommunications equipment such as core and metro routers supporting SyncE/SONET/SDH typically employ a distributed timing architecture:

- Redundant primary and secondary timing cards each use a low-bandwidth PLL with stable TCXO/OCXO reference. This is used to attenuate wander and jitter from incoming recovered clocks, and provide standards-compliant frequency stability during holdover.
- Fanout buffers distribute recovered clocks to individual line cards over a backplane.
- Line cards each contain a jitter-attenuating clock to remove backplane jitter and provide a clean clock to each of the PHY/SerDes devices.

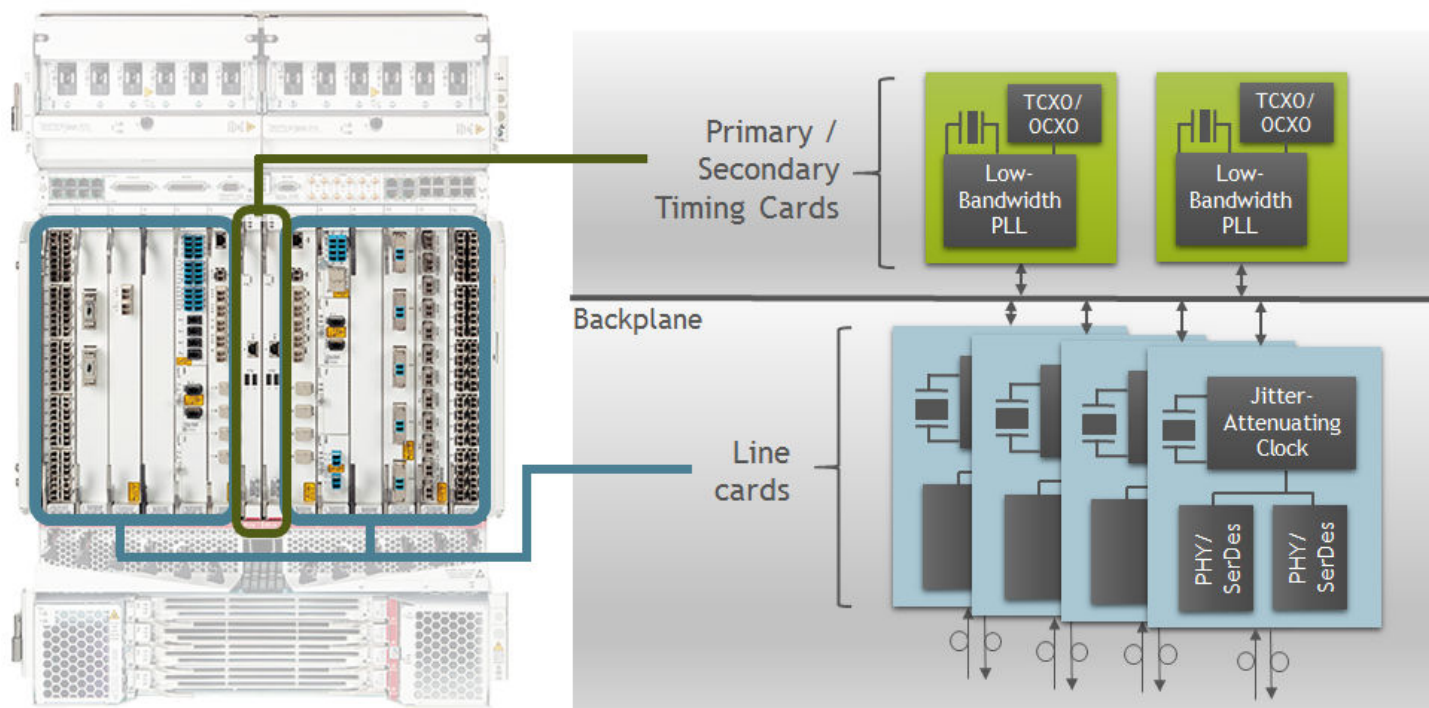


Figure 4.1. Distributed Timing Architecture

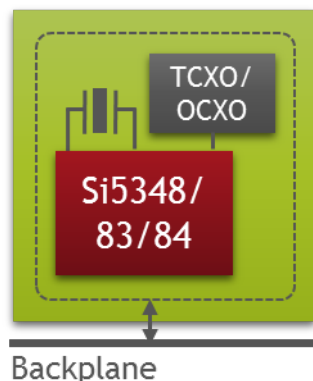
Some typical loop bandwidth requirements for timing cards are given below:

Table 4.1. Typical Loop Bandwidth Requirements

SONET (Telcordia)	SDH (ITU-T)	SyncE (ITU-T)	Loop Bandwidth
GR-253 Stratum 3E	G.812 Type III	—	0.001 Hz
GR-253 Stratum 3	G.812 Type IV	G.8262 EEC Option 2	<0.1 Hz
—	G.813 Option 1	G.8262 EEC Option 1	1 - 10 Hz

4.2 Recommended DSPLLs for Timing Card Designs

In order to support low PLL bandwidths and stable frequency performance, a TCXO or OCXO is required for timing card designs. In addition to the TCXO/OCXO, timing cards may need to support 1Hz/1PPS frequencies. For these reasons Skyworks recommends the use of dual-reference network synchronizers such as Si5348/83/84 for timing card designs.



- Phase noise performance above 100Hz is not affected by the TCXO/OCXO. Therefore a lower-cost TCXO/OCXO can be used and an additional jitter attenuator is not required on the PCB*
- Lower power consumption than competing devices
- A wide range of TCXO/OCXO output frequencies are supported: 5 to 250 MHz
- Support for 1 Hz/1 PPS output (Si5348) and 1 Hz/1 PPS input (Si5383/84)

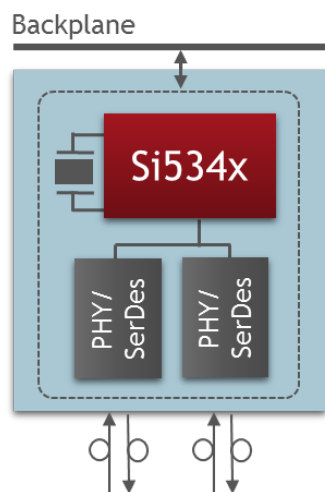
Figure 4.2. Si5348/83/84 Dual-Reference Clocks Recommended for Timing Card Designs

***Note:** Jitter performance is less critical for timing card clocks since each line card will have its own jitter attenuating clock. However, Si5348/83/84 can provide low-jitter clocks if required for other timing card devices without the need for an additional jitter attenuator.

4.3 Recommended DSPLLs for Line Card Designs

Line card clocks attenuate jitter (not wander) and provide switching between the primary and secondary timing card inputs. Loop bandwidths >10 Hz are typically used. The jitter performance of line card clocks is critical since these clocks are used as the input to PHY/SerDes components.

Skyworks recommends the use of single-reference jitter attenuators such as Si5342/4/5/6/7 for line card designs.



- Industry's lowest jitter, which is ideal for high-speed PHY/SerDes clocking
- MultiSynth fractional synthesizers offer the greatest frequency flexibility and 0ppm frequency synthesis error
- DSPLL technology is not susceptible to PLL crosstalk or power supply noise
- Lower power consumption than competing devices

Figure 4.3. Si5342/4/5/6/7 Recommended for Line Card Designs

If desired, an oscillator can be used in lieu of a crystal for the XA/XB input to Si534x but **it is necessary to use a low-jitter oscillator for line card designs**. As mentioned above, the output clock jitter of Si534x is dependent on the jitter performance of the oscillator.

4.4 Centralized Timing/"Pizza Box" Architecture

Smaller telecommunications equipment is often designed to fit in a 1U or 2U rack space. These designs may use a single PCB which must support all of the functions of the distributed timing architecture:

- A low-bandwidth PLL with stable TCXO/OCXO reference. This is used to attenuate wander and jitter from incoming recovered clocks, and provide standards-compliant frequency accuracy during holdover.
- Low-jitter PLL(s) and fanout buffers to provide clean clocks to each of the PHY/SerDes devices

If the low-bandwidth PLL does not provide sufficient jitter performance, an additional PLL can be used for jitter attenuation.

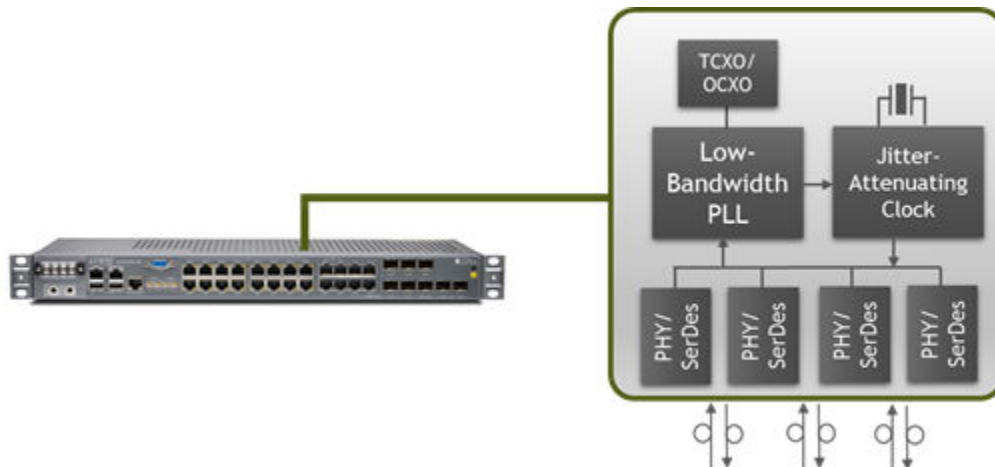
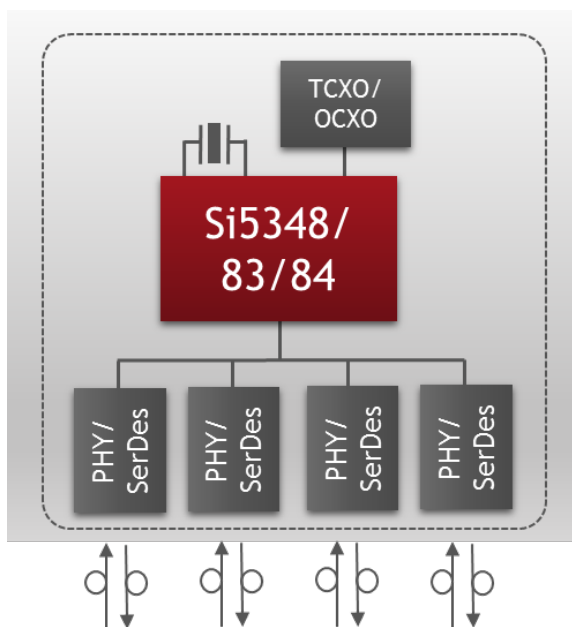


Figure 4.4. Centralized Timing / "Pizza Box" Architecture

4.5 Recommended DSPLLs for Centralized Timing/"Pizza Box" Architecture

As with timing cards, centralized timing designs require a TCXO or OCXO for low PLL bandwidths and stable frequency performance. 1Hz/1PPS frequencies may also be present. In addition, low-jitter clocks are needed for PHY/SerDes clocking. For these reasons Skyworks recommends the use of dual-reference network synchronizers such as Si5348/83/84 for "pizza box" designs.



- Industry's lowest jitter, which is ideal for high-speed PHY/SerDes clocking
- Phase noise performance above 100 Hz is not affected by the TCXO/OCXO. Therefore a low-cost TCXO/OCXO can be used and an additional jitter attenuator is not required on the PCB.
- DSPLL technology is not susceptible to PLL crosstalk or power supply noise
- Lower power consumption than competing devices
- A wide range of TCXO/OCXO frequencies are supported: 5 to 250 MHz
- Support for 1 Hz/1 PPS output (Si5348) and 1 Hz/1 PPS input (Si5383/84)

Figure 4.5. Si5348/83/84 Recommended for "Pizza Box" Designs

4.6 Wireless Base Station/BBU/eNodeB Applications

Wireless base station applications often have a distributed architecture similar to section 4.1 [Distributed Timing Architecture](#) above. “Control boards” are similar to timing cards and the clock devices must attenuate wander and jitter, and provide a stable frequency reference. “Baseband boards” are similar to line cards and the clock devices must switch between redundant control boards, attenuate backplane jitter and provide clean clocks to PHY/SerDes devices. Phase alignment of output clocks may also be needed on baseband boards.

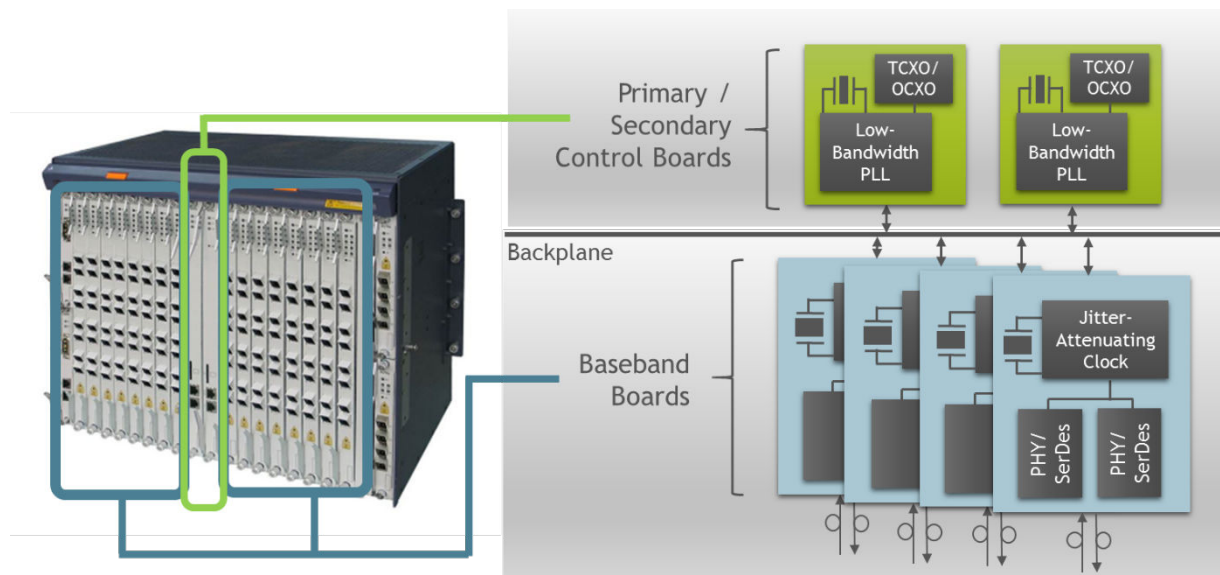
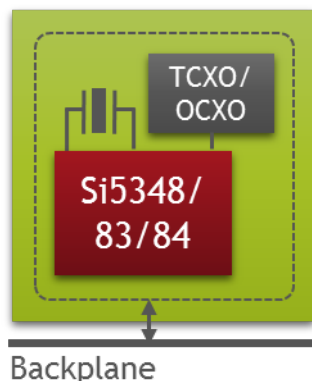


Figure 4.6. Wireless Base Station / BBU / eNodeB Architecture

4.7 Recommended Clocks for Wireless Base Station/BBU/eNodeB Applications

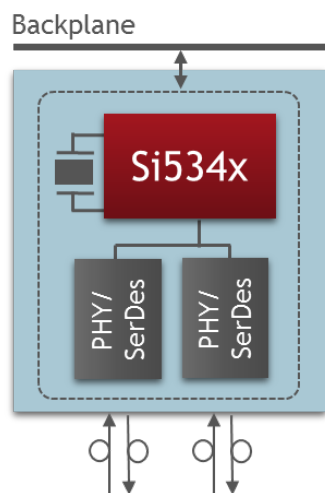
As with timing cards, Skyworks recommends the use of dual-reference network synchronizers such as Si5348/83/84 for wireless base station control board designs. The Si5348/83/84 offers superior performance with a stable TCXO/OCXO reference, and supports for 1 PPS/1 Hz frequencies.



- Phase noise performance above 100Hz is not affected by the TCXO/OCXO. Therefore a low-cost TCXO/OCXO can be used and an additional jitter attenuator is not required on the PCB.
- A wide range of TCXO/OCXO output frequencies are supported: 5 to 250 MHz
- Support for 1Hz/1PPS output (Si5348) and 1Hz/1PPS input (Si5383/84)

Figure 4.7. Si5348/83/84 Recommended for Wireless Base Station Control Boards

Skyworks recommends the use of single-reference jitter attenuators such as Si5342/4/5 for wireless baseband boards. These devices offer the industry's best jitter performance and can provide low input-to-output skew when used in zero delay mode. The output delay/skew is also adjustable which can compensate for different PCB trace delays. (Note Si5346/7 do not offer zero delay mode or adjustable output delay.)



- Industry's lowest jitter, which is ideal for high-speed PHY/SerDes clocking
- Low input-to-output skew (with zero delay mode), and adjustable output skew
- MultiSynth fractional synthesizers offer the greatest frequency flexibility and 0ppm frequency synthesis error
- DSPLL technology is not susceptible to power supply noise
- Lower power consumption than competing devices

Figure 4.8. Si5342/4/5 Recommended for Wireless Base Station Baseband Boards

4.8 Wireless Radio Interface (RRH and RRU) Applications

Radio interface devices for wireless infrastructure, sometimes referred to as remote radio head (RRH) or remote radio unit (RRU), typically connect to base stations with a Common Public Radio Interface (CPRI) fronthaul link. The RRH/RRU then contains a CPRI receiver and the radio interface:

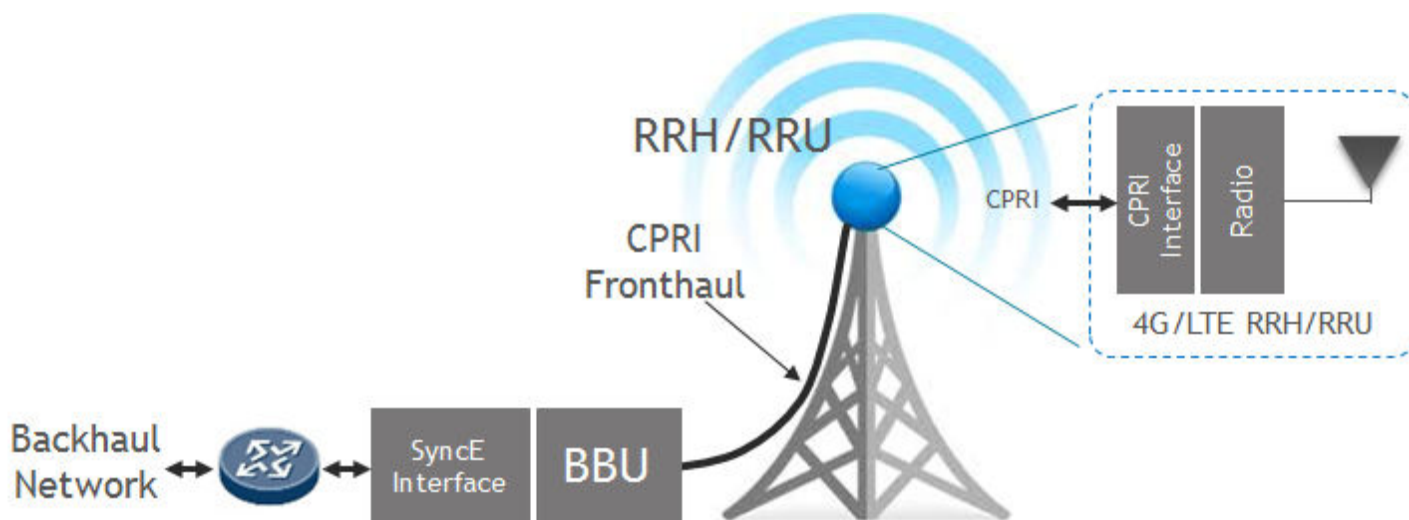


Figure 4.9. Traditional 4G/LTE Wireless Fronthaul with CPRI

Emerging wireless infrastructure deployments including Cloud-RAN and 5G are now consolidating base station and radio interface functionality into a single unit, while adding IEEE1588 for phase synchronization:

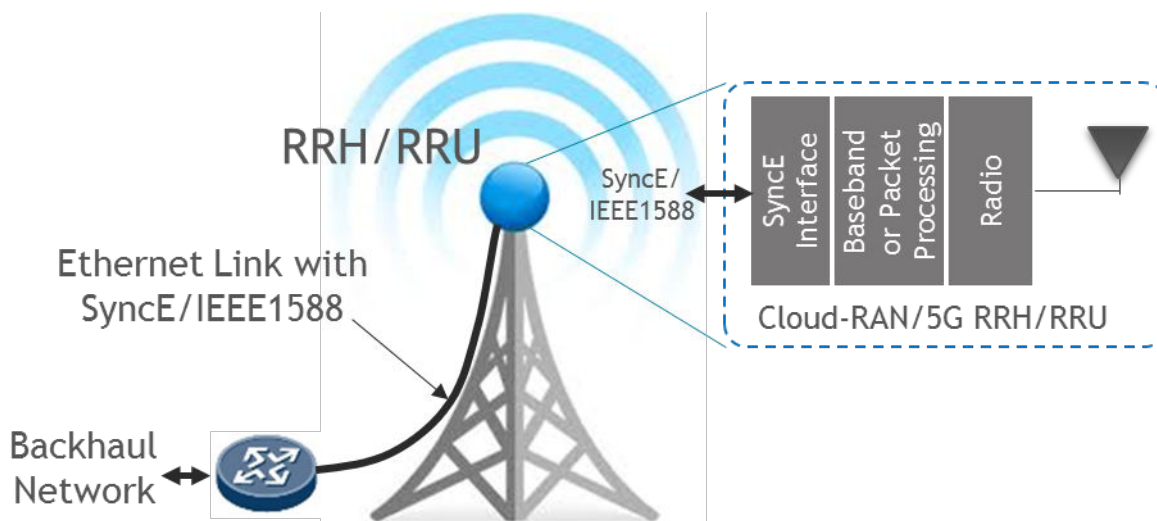


Figure 4.10. Emerging Cloud-RAN / 5G Radio Interface

As a result, CPRI fronthaul links are no longer required for Cloud-RAN/5G, and SyncE/1588 is connected directly to the RRH/RRU. This presents a challenge to clock tree design due to dissimilar requirements of baseband and radio interface clocks:

Table 4.2. Typical Radio Interface vs. SyncE/1588 Baseband Clock Requirements

Specification	Typical SyncE/1588 Baseband Clock Requirements	Typical Radio Interface Clock Requirements
PLL Bandwidth	Very low <10 Hz	100 Hz
Stable Frequency Reference	Yes, TCXO/OCXO	No
Output Frequencies	Typically multiples of 6.25 MHz, including 156.25 MHz, 125 MHz	Typically multiples of 480 kHz, including 307.2 MHz, 245.76 MHz
1 PPS/1 Hz Support	Yes	No
Output Clock Phase Alignment and Adjustment (JESD204B)	No	Yes, JESD204B

4.9 Recommended Clocks for Traditional 4G/LTE Wireless Radio Interface (RRH and RRU) Applications

4G/LTE RRH/RRU designs need a jitter attenuating clock with low phase noise that supports JESD204B clock phase alignment. Skyworks' Si5380 device is designed for these applications:

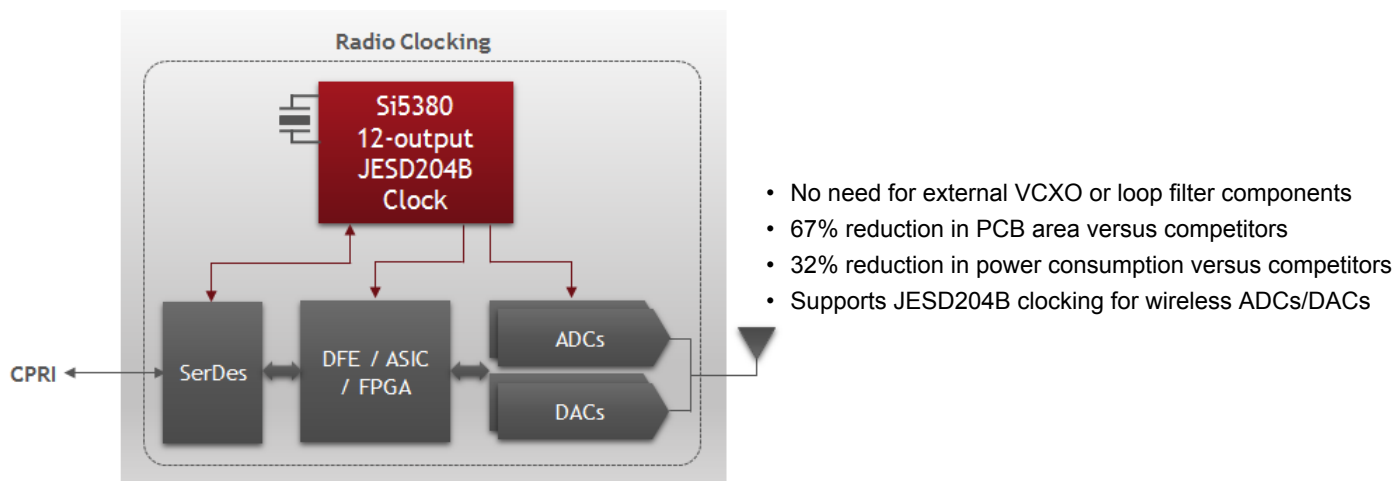


Figure 4.11. Si5380 Recommended for 4G/LTE RRH/RRU Designs

4.10 Recommended Clocks for Cloud-RAN/5G Wireless Radio Interface (RRH and RRU) Applications

Given the dissimilar requirements for the SyncE/1588 baseband clocks and the radio interface clocks, Skyworks recommends two clock devices for Cloud-RAN/5G RRH/RRU designs. The Si5348/83/84 should be used for the baseband in order to support the low PLL bandwidth and stable TCXO/OCXO reference. For the radio interface the Si5380 should be used, as it provides the lowest close-in phase noise as well as JESD204B clock phase alignment.

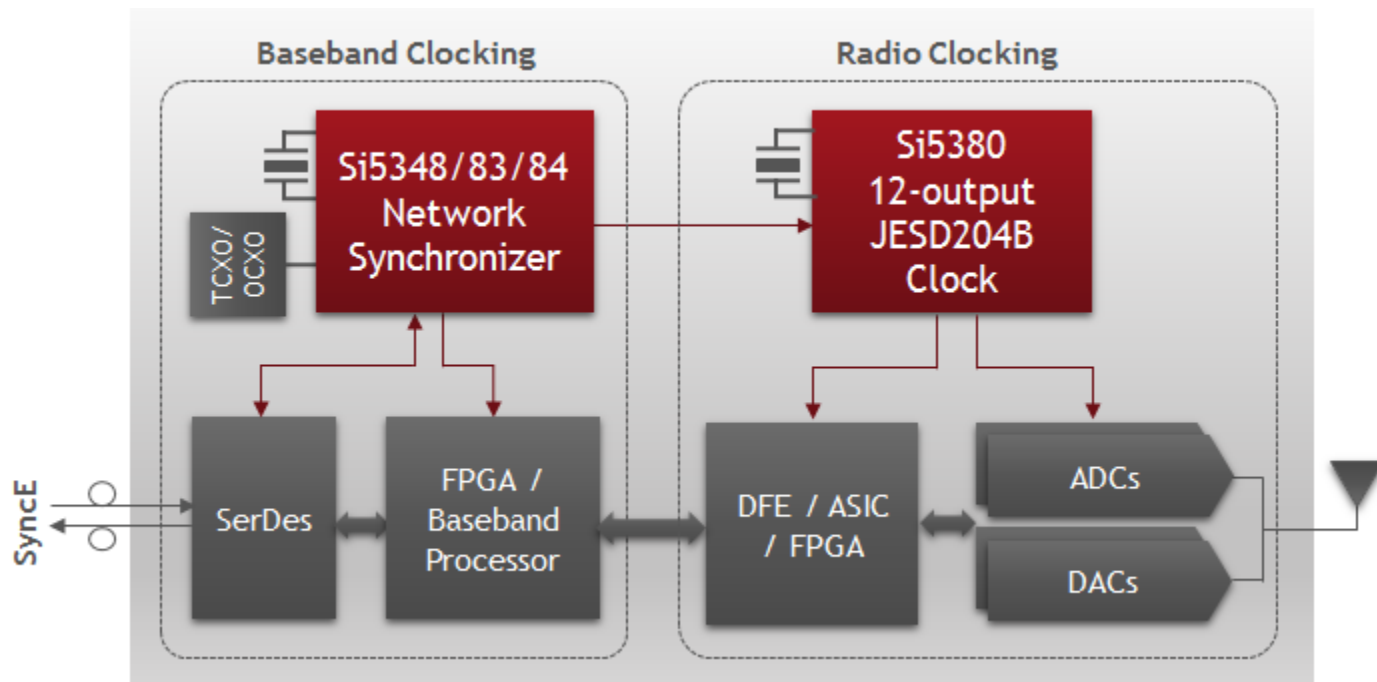


Figure 4.12. Radio Interface Clocking for Cloud-RAN / 5G

This arrangement offers advantages for both the baseband clock tree and the radio clock tree:

Baseband Clock Advantages with Si5348/83/84:

- Phase noise performance above 100 Hz is not affected by the TCXO/OCXO. Therefore a lower-cost TCXO/OCXO can be used and an additional jitter attenuator is not required on the PCB.
- A wide range of TCXO/OCXO output frequencies are supported: 5 to 250 MHz
- Support for 1 Hz/1 PPS output (Si5348/83/84) and 1 Hz/1 PPS input (Si5383/84)

Radio Clock Advantages with Si5380:

- No need for external VCXO or loop filter components
- 67% reduction in PCB area versus competitors
- 32% reduction in power consumption versus competitors
- Supports JESD204B clocking for wireless ADCs/DACs

5. Summary and Selection Guide

With both single-reference and dual-reference clocks, Skyworks Si534x/8x devices provide flexible options to meet the needs of today's synchronization designs. The selection guide below summarizes Skyworks' recommendations for various application types.

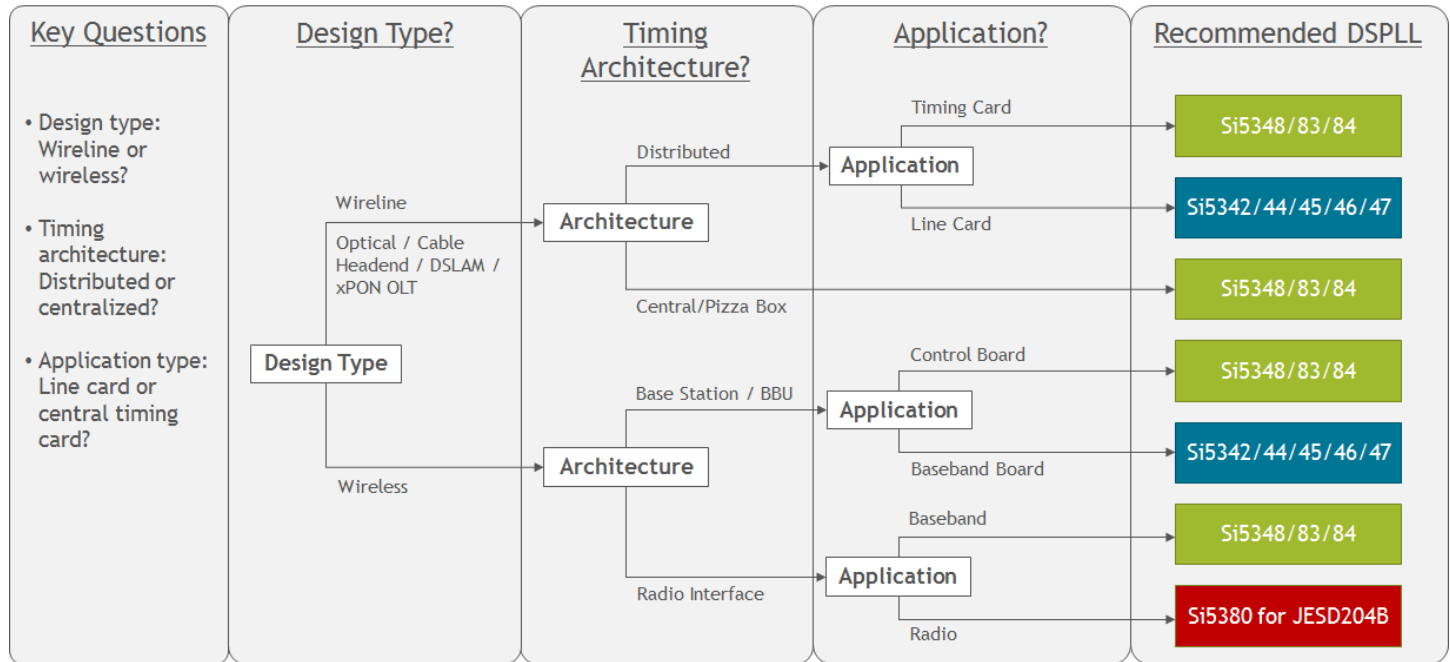


Figure 5.1. Synchronization Clock Selection Guide



ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

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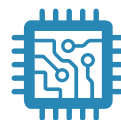
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